AMENDMENTS TO THE CLAIMS

This listing of claims will replace all prior versions and listings of claims in the application:

LISTING OF CLAIMS:

1. (Currently Amended) A method of transmitting data traffic received from a plurality of prioritized sources, wherein the method comprises:

(a) setting the highest priority source with data traffic waiting for transmission as a current transmission source;

(b) transmitting the data traffic from the current transmission source until completion while monitoring the remaining sources for waiting data traffic, wherein if traffic is detected from a source with a higher priority than the current transmission source, completing transmission of the minimum transmittable element from the current transmission source prior to starting transmission of data traffic from the source with higher priority;

(c) upon completion of the transmission of data traffic from the current transmission source, going to step (a),

wherein the data traffic as received from said plurality of prioritized sources includes control data, and step (b) further comprises incorporating into said control data at least one reassembly indicator for use in reassembling the data traffic upon receipt, ~~said~~and wherein all reassembly ~~indicator being~~indicators needed for reassembling the data traffic upon receipt are incorporated into said control data in such a way as to not increase the amount of said control data already present in said data traffic.

2. (*Cancelled*).

3. (Previously Presented) The method according to claim 1, in which the minimum transmittable element for data traffic of asynchronous and bit-synchronous protocols is a bit.

4. (Previously Presented) The method according to claim 1, in which the minimum transmittable element for data traffic of slot-synchronous protocols is a slot.

5. (Previously Presented) A method of reassembling a number of traffic streams interleaved within a data stream into a respective output queue for each traffic stream, wherein the method comprises:

(a) clearing the output queues and selecting a first output queue for receiving the data stream;

(b) passing the data stream to the selected output queue while monitoring the data stream, and going to step (c) upon detection of a start indicator of a new traffic stream different from the traffic stream currently being received, wherein the start indicator of the new traffic stream is located after a minimum transmittable element of the currently received traffic stream, and going to step (d) if the end of a traffic stream is determined, wherein the start and end of said traffic streams are determined from at least one reassembly indicator incorporated into control data contained within the traffic streams without increasing the amount of control data already present in said traffic streams prior to interleaving;

(c) selecting a further output queue to receive the new traffic stream and going to step (b); and

(d) if a memory stack contains one or more identifiers of output queues, retrieving the top identifier from the stack, selecting the output queue corresponding to the identifier to resume receiving said currently received traffic stream and going to step (b), otherwise going to step (a).

6. (Currently Amended) A switch comprising:

a plurality of memory devices defining queues for receiving traffic to be switched, wherein each queue is associated with a predetermined priority classification, and

a processor for controlling the transmission of traffic from the queues to an output, wherein the processor monitors the queues to determine whether traffic has arrived at a queue having a higher priority classification than the queue from which traffic is currently being transmitted, and if traffic arrives in a queue that has a higher priority than the queue from which traffic is currently being transmitted, the processor suspends the current transmission after transmission of the minimum transmittable element from the lower priority queue and transmits traffic from the higher priority queue, and subsequently resumes the suspended transmission after completing transmission of the higher priority traffic, wherein the traffic received by said memory devices includes control data and, prior to transmission, the processor modifies said control data without increasing the amount of said control data to comprise whatever reassembly indicators are needed, including at least one reassembly indicator, for ~~use in~~ reassembling the traffic upon receipt.

7. (*Cancelled*).

8. (Previously Presented) The switch according to claim 6, wherein the reassembly indicators comprise different start and end indicators for each cell or packet in the traffic.

9. (Previously Presented) The switch according to claim 6, wherein the reassembly indicators comprise start and length indicators for each cell or packet in the traffic.

10. (Previously Presented) The switch according to claim 6, wherein the reassembly indicators indicate the queue's priority classification.

11. (Previously Presented) The switch according to claim 9, wherein the processor adapts each packet or cell in the traffic received from the queues to include an indication of the queue's priority classification.

12. (Previously Presented) The switch according to claim 6, wherein the processor stores predetermined details of interrupted traffic transmissions and their respective queues in one of the memory devices and retrieves the details for use in resuming the interrupted transmission once the interrupting transmission is completed.

13. (Previously Presented) The switch according to claim 6, further comprising a number of outputs, wherein the processor transmits traffic to an appropriate output depending upon the traffic's destination address.

14. (Previously Presented) The switch according to claim 6, wherein the minimum transmittable element for traffic of asynchronous and bit-synchronous protocols is a bit.

15. (Previously Presented) The switch according to claim 6, wherein the minimum transmittable element for traffic of slot-synchronous protocols is a slot.

16. (Previously Presented) A switch comprising an input from which a data stream is received, the data stream comprising interleaved portions of different traffic streams, a number of output queues and a processor configured to separate the data stream into respective ones of the output queues for reassembly of individual traffic streams from the data stream, wherein the processor monitors the data stream while routing a first traffic stream to a first output queue until the processor detects a start indicator of a new interleaved portion of a second traffic stream, wherein the processor routes the new interleaved portion of said second traffic stream to a second output queue until the end of the new interleaved portion of the second traffic stream is determined, thereafter the processor routes the first data stream to the first output queue, or until another start indicator of another new interleaved portion of a traffic stream is detected within the data stream, wherein the processor routes the another new interleaved portion to a third output queue, wherein said start and end of said interleaved portions of said traffic streams are

determined from at least one reassembly indicator incorporated into control data contained within said interleaved portions of traffic streams in such a way as to not increase the amount of control data above the amount already included in said traffic streams prior to interleaving.

17. (*Cancelled*).

18. (Previously Presented) The switch according to claim 16, in which the end of an interleaved portion of traffic is determined in dependence on a portion length indicator within the interleaved portion of traffic.

19. (Previously Presented) The switch according to claim 16, in which the end of an interleaved portion of traffic is determined from end indicator within the data stream.

20. (Previously Presented) The switch according to claim 16, in which each interleaved portion of traffic comprises a priority indicator, wherein the end of an interleaved portion of traffic is determined from a drop in level of the priority indicator.

21. (Previously Presented) The switch according to claim 16, in which each interleaved portion of traffic comprises a priority indicator, wherein a start indicator comprises a rise in the level of the priority indicator.

22. (Previously Presented) The switch according to claim 16, in which the processor operates as a state machine.

23. (Previously Presented) A telecommunications network comprising a switch as claimed in claim 6.*

24. (Previously Presented) A computer program product comprising a number of computer executable instructions for executing the steps of claim 1.